**19EC22P3 – DIGITAL SYSTEM DESIGN LAB USING VHDL**

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| **Course Category:** | Program Core | **Credits:** | 2 |
| **Course Type:** | Practical | **Lecture-Tutorial- Practice:** | 0 - 0 – 3 |
| **Prerequisite:** | Switching theory & logic design, Digital design and digital IC’s | **Sessional Evaluation:****External Evaluation :****Total Marks:** | 4060100 |
| **Course****Objectives** | Students undergoing this course are expected to understand: |
|  1. How to write VHDL programs of different digital circuits. 2. How to simulate the VHDL programs of different digital circuits.  |
| **Course Outcomes** | Upon successful completion of the course , the students will be able to: |
| CO1 | Write and simulate the various logic gates by using VHDL. |
| CO2 | Write and simulate the adders and subtractors by using VHDL. |
| CO3 | Verify the truth table of various digital circuits and IC’s. |
| CO4 | Design the various digital circuits. |
| CO5 | Write and simulate the various counters by using VHDL. |
| CO6 | Write and simulate the various registers by using VHDL. |
| **Course****Content** | Minimum of **TEN** experiments to be completed out of the following:**LIST OF EXPERIMENTS**1. Logic Gates
2. Full Adder & Full Subtractor
3. 3 to 8 Decoder
4. 8 to 3 Encoder
5. 4 bit Comparator
6. 8x1 Multiplexer
7. 1x4 Demultiplexer
8. D Flip-Flop
9. Decade Counter
10. Shift Register
11. BCD to 7-segment display code converter
12. 3 bit up/down Ripple counter
13. 2 bit synchronous counter
14. Bi-directional shift register
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| Contribution of Course Outcomes towards achievement of Program Outcomes  |
|  | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 | PSO1 | PSO2 |
| CO1 | 3 | 3 | 2 | - | 1 | - | - | - | - | - | 2 | 2 | 3 | 3 |
| CO2 | 3 | 3 | 2 | - | 1 | 1 | - | - | - | - | 2 | - | 3 | 3 |
| CO3 | 3 | 3 | 3 |  - |  1 |  - |  - |  - |  - |  - |  2 |  2 |  3 |  3 |
| CO4 | 3 | 3 | 2 | - | 1 | 1 | - | - |  - | - | - | - | 3 | 3 |
| CO5 | 3 | 3 | 2 | - | 1 | - | - | - | - | - | - | 2 | 3 | 3 |
| CO\6 | 3 | 3 | 2 | - | 1 | - | - | - | - | - | 2 | 2 | 3 | 3 |